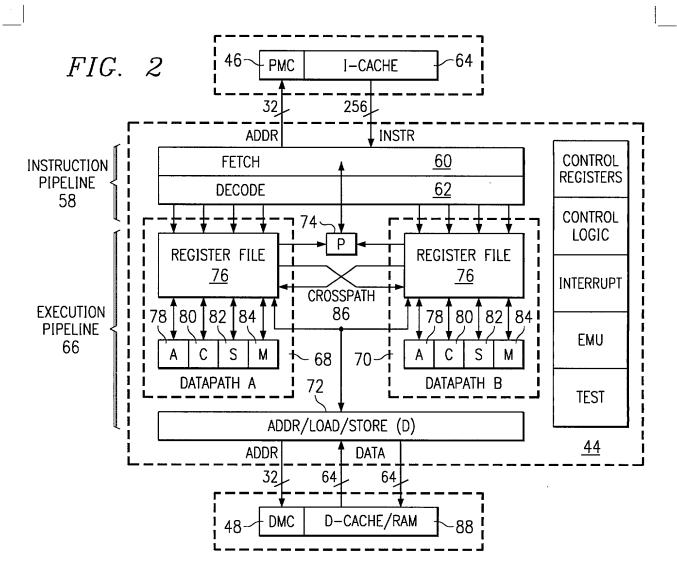


FIG. 1



UNIT		REGISTER FILE ACCESS		
GROUP	DE PATIONS 1		ALTERNATIVE DATAPATH	
A	GENERAL ARITHMETIC BOOLEAN AND CONTROL REGISTER ACCESS	R/W	R	
С	- COMPARE, SHIFT, BOOLEAN - ARITHMETIC: ADD, SUB	R/W	R	
S	-SHIFT, ROTATE, EXTENDED BOOLEAN -ARITHMETIC: ADD, SUB	R/W	R	
М	-MULTIPLY -ARTHMETIC: ADD, SUB	R/W	R	
D	- LOAD - STORE - ADDRESS COMPUTATION	W TO BOTH R FROM BOTH R/W BOTH		
Р	- BRANCH	R FRO	и вотн	

FIG. 3

R=READ, W=WRITE

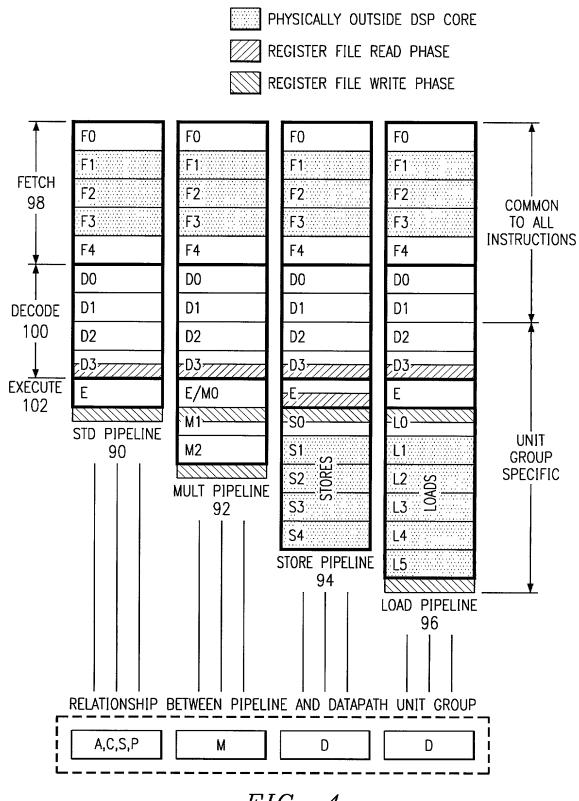


FIG. 4

STAGE	FUNCTION
F0	SEND PC TO PROGRAM MEMORY CONTROLLER. LDIP ASSIGNED.
F1	CACHE BLOCK SELECT.
F2	ADDRESS PHASE OF INSTRUCTION CACHE ACCESS.
F3	DATA PHASE OF INSTRUCTION CACHE ACCESS.
F4	FETCH PACKET SENT TO DSP.

STAGE	FUNCTION
DO	DETERMINE VALID INSTRUCTIONS IN CURRENT FETCH PACKET.
D1	SORTS INSTRUCTIONS IN EXECUTE PACKET ACCORDING TO DESTINATION UNITS.
D2	INSTRUCTIONS SENT TO DESTINATION UNITS. CROSSPATH REGISTER READS OCCUR.
D3	UNITS DECODE INSTRUCTIONS. REGISTER FILE READ (2ND PHASE).

## FIG. 5a

FIG. 5b

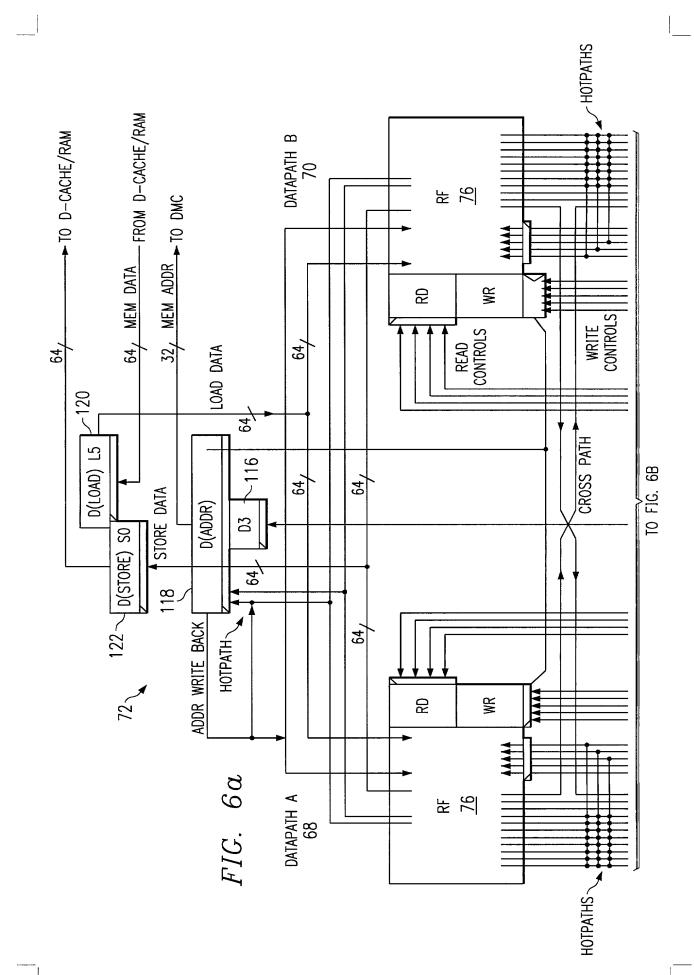
UNIT	STAGE	FUNCTION
NON M UNIT	E	EXECUTION OF OPERATION BEGINS AND COMPLETES. FULL RESULT AVAILABLE AT END OF CYCLE.
M UNIT	МО	EXECUTION OF MULTIPLY OPERATION BEGINS. (OR, NON-MULTIPLY OPERATION BEGINS AND COMPLETES.)
M UNIT	М1	MULTIPLY OPERATION CONTINUES. (OR, NON-MULTIPLY RESULT WRITTEN TO REGISTER FILE (PHASE 1).)
M UNIT	M2	MULTIPLY OPERATION COMPLETES.

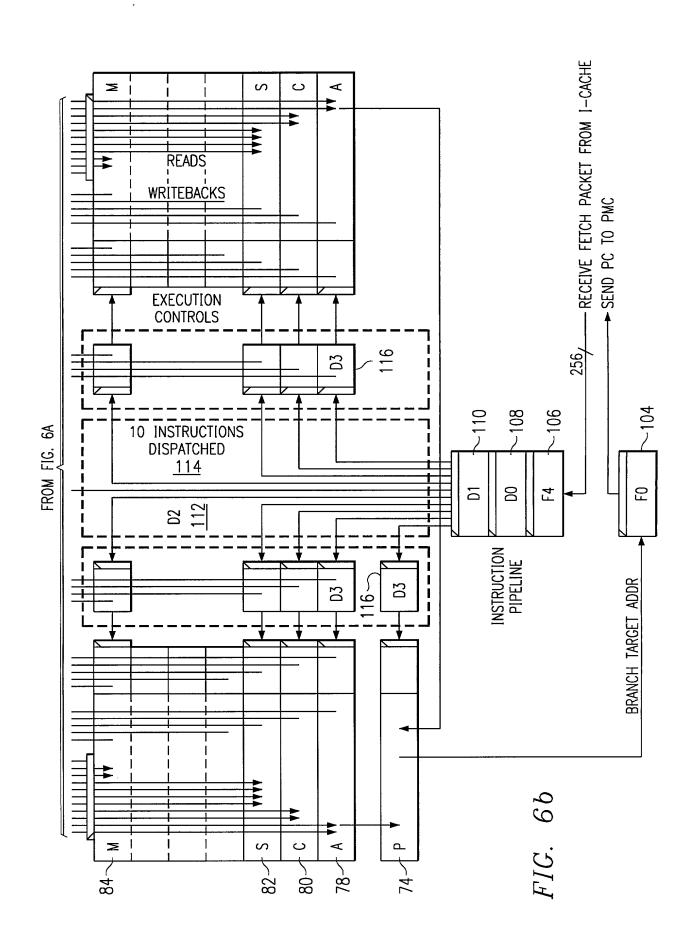
## FIG. 5c

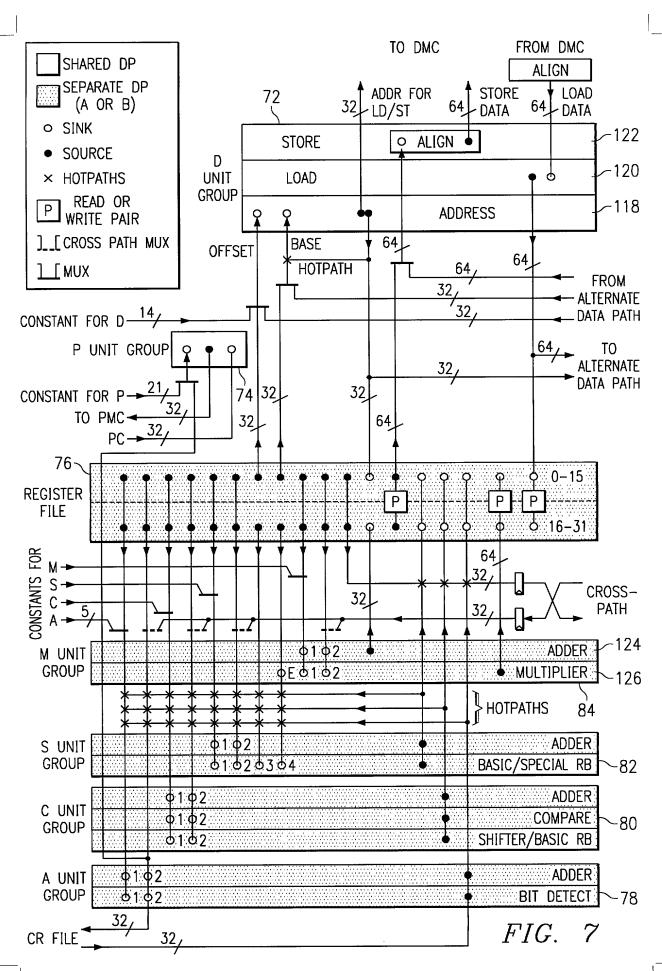
STAGE	FUNCTION
E	ADDRESS GENERATION OCCURS. REGISTER FILE ACCESS FOR READ DATA.
LO	LOAD ADDRESS GENERATED DURING E IS SENT TOWARDS THE DMC.
L1	ADDRESS DECODE, TC ARBITRATION, TAG COMPARES.
L2	ADDRESS DECODE, TC ARBITRATION, TAG COMPARES.
L3	ADDRESS PHASE OF DATA CACHE ACCESS.
L4	DATA PHASE OF DATA CACHE ACCESS.
L5	64-BIT DATA SENT TO DSP.

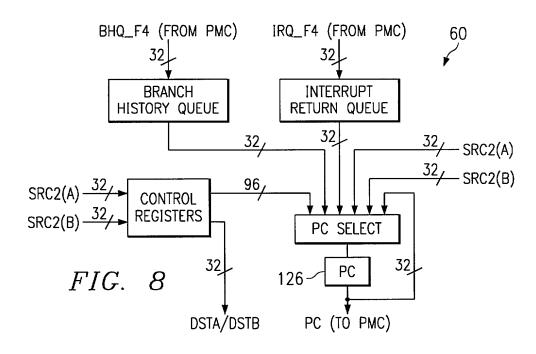
## FIG. 5d

STAGE	FUNCTION
E	ADDRESS GENERATION OCCURS. REGISTER FILE ACCESS FOR WRITE DATA.
S0	ADDRESS SENT TO DMC.
S1	ADDRESS DECODE IN DMC. WRITE DATA ALIGNMENT.
S2	TAG COMPARE IN DMC. WRITE DATA SENT TO DMC.
S3	ADDRESS PHASE IN DATA CACHE.
S4	DATA PHASE IN DATA CACHE.



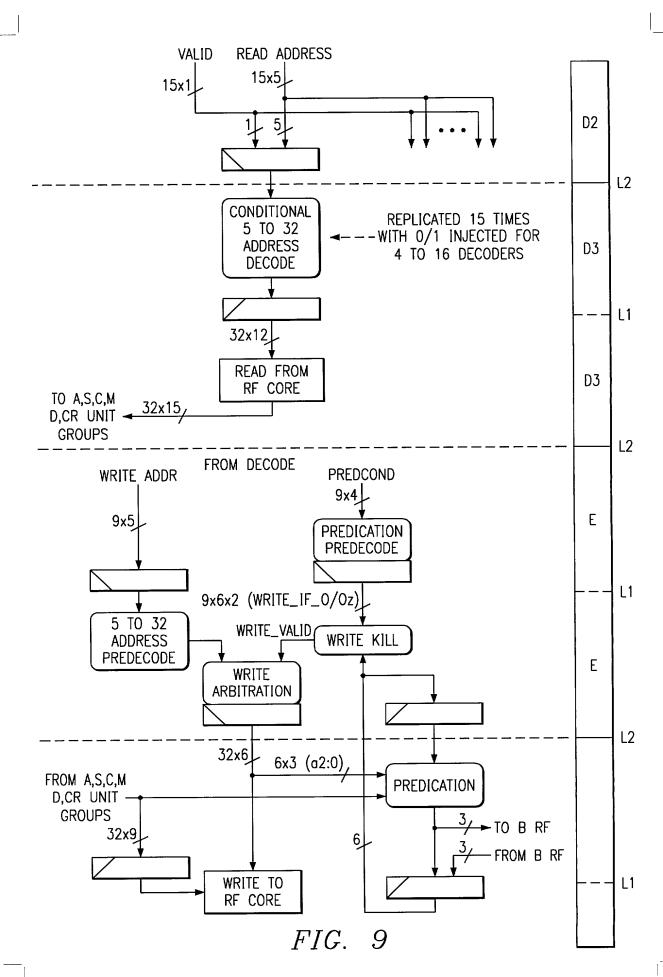


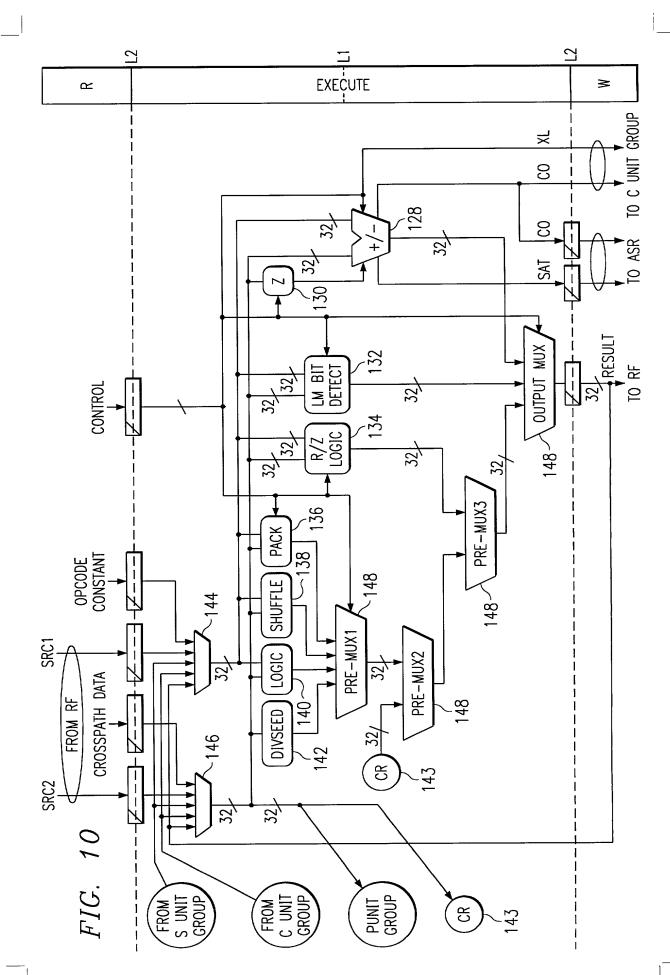


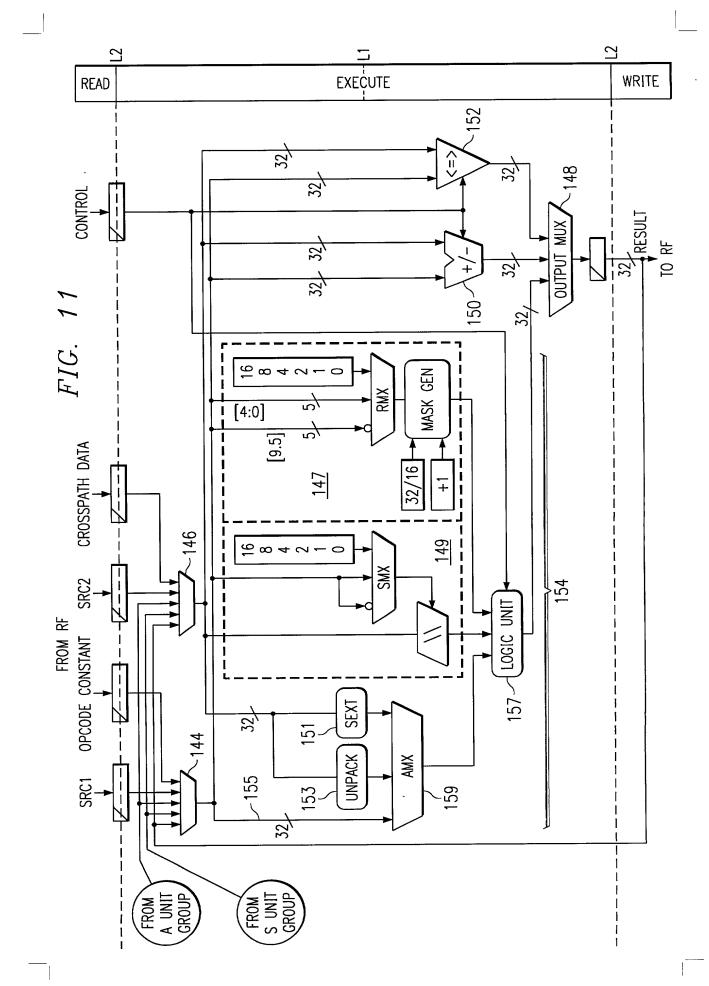


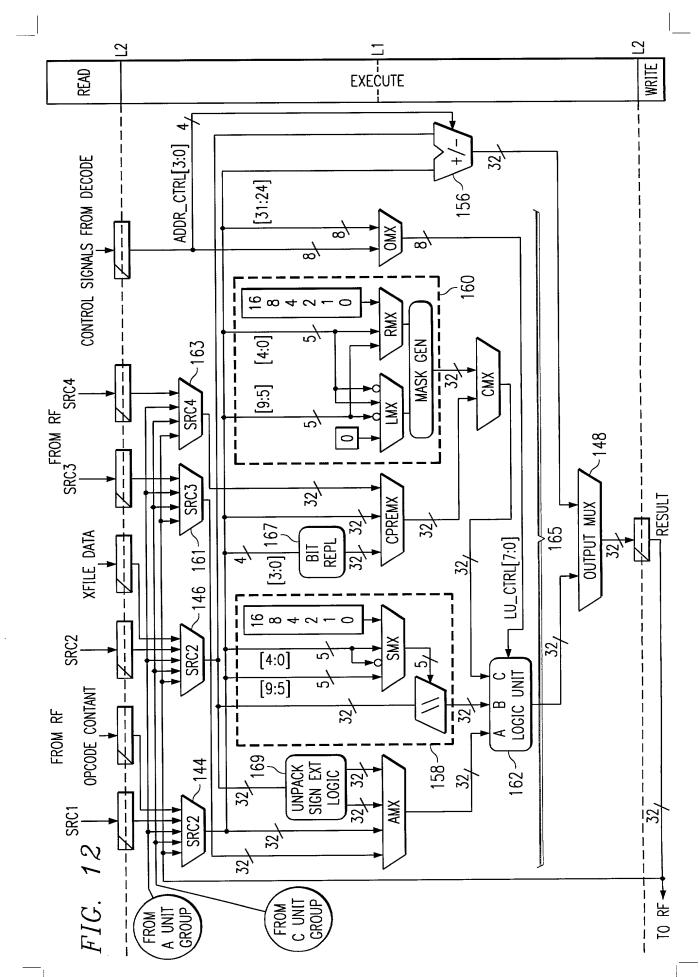
	[PREDIC	ATION REG] IN	ISTRUCTION_MN	NEMONIC	.UNIT-DATAPATH-	CROSSPAT	H OP1, OP2, DST	Г
WHERE:    TO BE SCHEDULED IN PARALLEL WITH PRECEDING INSTRUCTION(S)    PREDICATION REG   = REGISTER CONTAINING PREDICATION VALUE   JUNIT								
	UNIT ASSEMBLY NOTATION		NOTATIONS	ASSEMBLY		WITH		
	GROUP	DATAPATH A	DATAPATH B	EXAMPLES		CROSSPATH		
	A	.A1	.A2	ADD SUB	.A1 A1,A2,A3 .A2 B1,B2,B3	ADD SUB	.A1X A1,B2,A3 .A2X B1,A2,B3	
	С	.C1	.C2		.C1 A1,A2,A3 .C2 B1,B2,B3		.C1X A1,B2,A3 .C2X B1,A2,B3	
	S	.S1	.S2	SHL SHL	.S1 A1,A2,A3 .S2 B1,B2,B3	SHL SHL	.S1X A1,B2,A3 .S2X B1,A2,B3	
i	М	.M1	.M2	MPY MPY	.M1 A1,A2,A3 .M2 B1,B2,B3	MPY MPY	.M1X A1,B2,A3 .M2X B1,A2,B3	
	D	.D		LDB STB ADDAH	.D *A8,A12 .D A8,*A12 .D A8,A2,B1		n/a	
	Р	.P		В	A8		n/a	

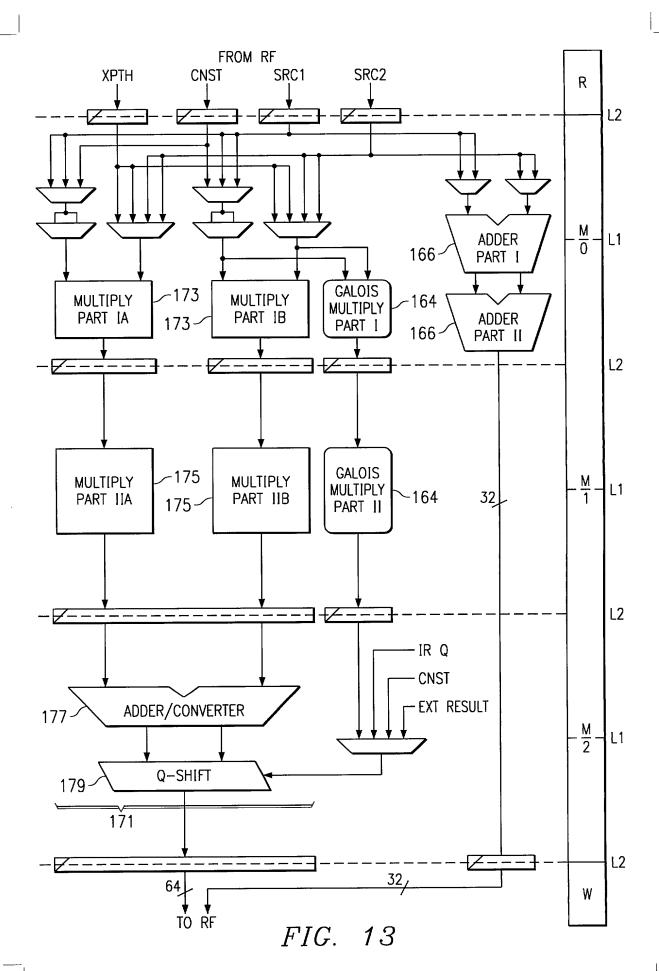
FIG. 15

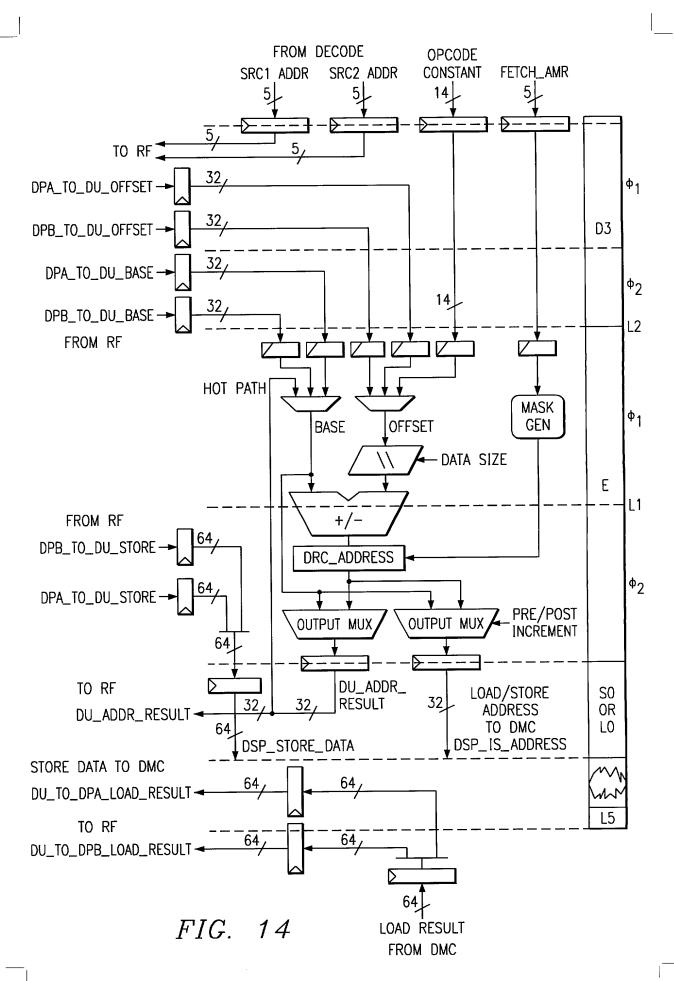


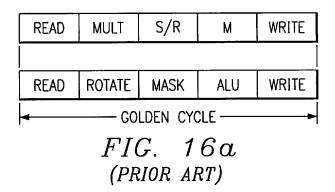


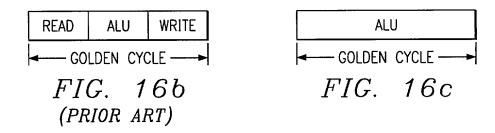


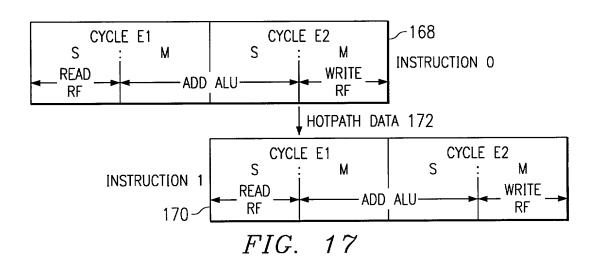


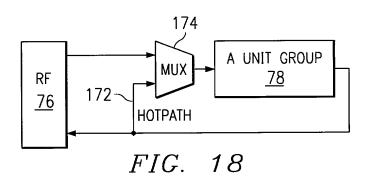


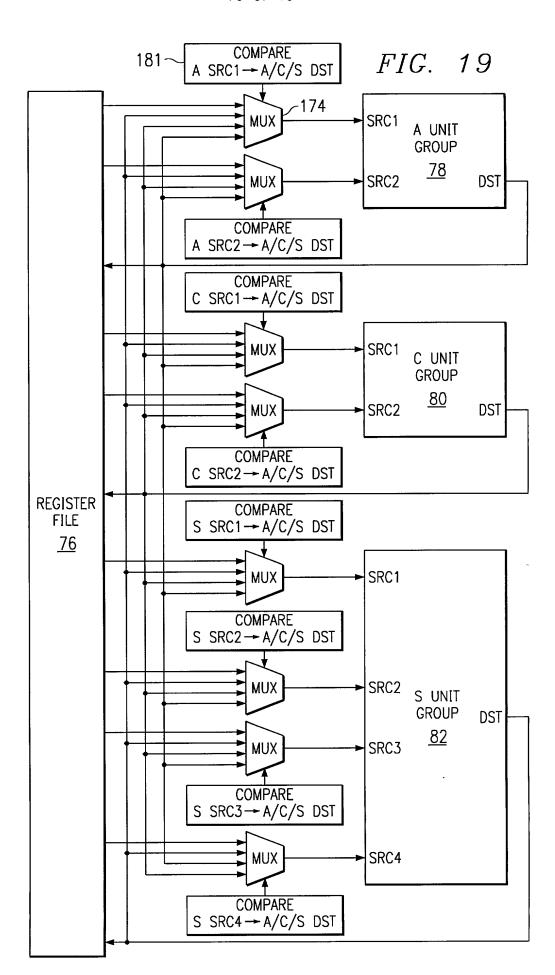












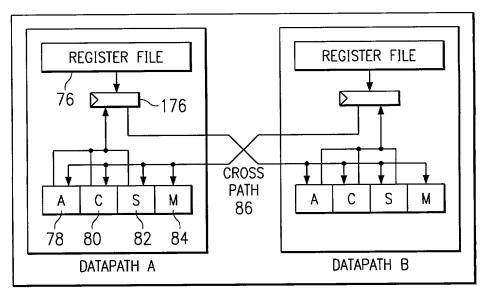
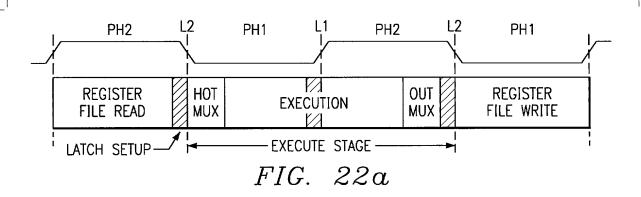
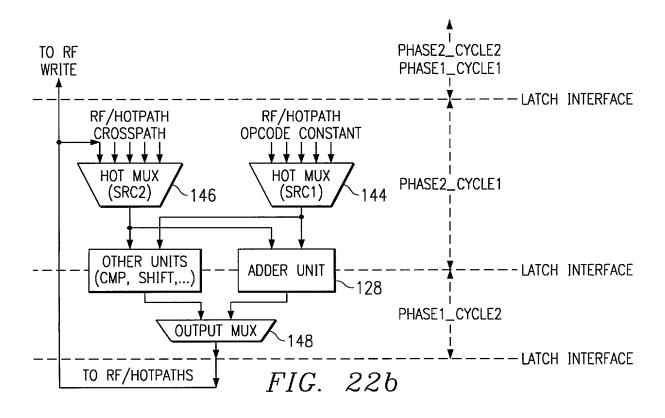


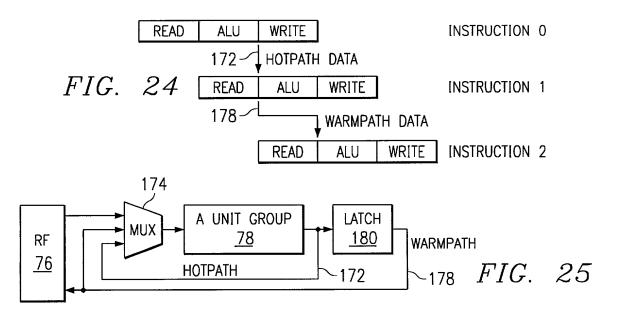
FIG. 20

		SOURCE(S) DATA PATH						
		A,C,S	M (ADD)	M (MUL)	D (LOAD)	D (STORE)	D (ADDR)	
	A,C,S	0	1	3	7	_	1	
	М	1	1	3	7	_	1	
	D (LOAD)	_	_	_	<b>–</b>	0	<u></u>	
SINK(S) IN	D (STORE)	0	0	2	6	_	0	
SAME DATAPATH	D (ADDR:BASE)	1	-	3	7	_	0	
	D (ADDR:OFFSET)	1	_	3	7	_	1	
	Р	0	1	3	7	_	1	
	PREDICATION	0	_	2	6	_	0	
SINK(S) IN	A,C,S	1	2	4	8	_	2	
OPPOSITE	М	1	2	4	8	-	2	
DATAPATH	PREDICATION	0		2	6	_	0	

FIG. 21







READ PHASE WRITE PHASE
EXECUTE STAGE

INSTRUCTION 1	ADD	REG1,	REG2,	REG3	_
INSTRUCTION 2	ADD	REG3,	REG4,	REG5	

